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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,037	06/19/2003	Hannu Huotari	ASMMC.047AUS	8258

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/601,037	HUOTARI, HANNU
	Examiner	Art Unit
	Christy L. Novacek	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-24 and 27-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-24 and 27-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed June 6, 2005 and the request for continued examination filed July 5, 2005.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 6, 2005 has been entered.

Response to Amendment

The limitations added to claims 15 and 42 are sufficient to overcome the rejections of claims 15-24, 27-38 and 40-42 under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417) in view of Elers et al. (WO 01/29893 A1) and Pomarede et al. (US 20020098627) and the rejections of claim 39 under 35 U.S.C. 103(a) as being unpatentable over Bai et al. in view of Elers et al., Pomarede et al. and further in view of Chang et al. (US 6,660,630). Therefore, those rejections are hereby withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 15-24, 27, 28, 33-38 and 40-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417, previously cited) in view of Matsuse et al. (US 6,861,356).

Regarding claim 15, Bai discloses depositing a gate dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the gate dielectric layer such that it overlies both the first and second regions, and forming first and second gate electrode layers (130/135) over the first -and second regions, respectively (col. 3, ln. 17 - col. 4, ln. 64). Bai states that the function of the barrier layer is to "inhibit interaction between the gate dielectric and the gate electrode." Thus, the barrier layer must be able to keep metal atoms in the gate electrode from diffusing into the underlying gate dielectric.

Bai does not disclose by what method the gate dielectric layer and barrier layer may be deposited. Like Bai, Matsuse discloses depositing a gate barrier layer onto a gate dielectric layer. Matsuse teaches that it is advantageous to use atomic layer deposition (ALD) to deposit the gate dielectric layer and barrier layer because the ALD process allows the layers to be more densified than they would be if deposited by other methods and also allows the layers to be formed such that they are ultra-thin (Fig. 13A; col. 7, ln. 8-13; col. 19, ln. 20-52). Matsuse does not disclose that the barrier layer is a nanolaminate. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the gate dielectric layer and barrier layer of Bai using an ALD process because Matsuse teaches that using ALD provides the benefits of forming densified, ultra-thin layers.

Regarding claim 16, Bai discloses that one of the regions is a PMOS region and the other region is an NMOS region (col. 3, ln. 8-16).

Regarding claim 17, Bai discloses the first and second gate electrode layers are adjacent (Fig. 7).

Regarding claim 18, Bai discloses that the first gate electrode layer includes a first gate electrode material and the second gate electrode includes a second gate electrode material (col. 3, ln. 55-65; col. 4, ln. 41-53).

Regarding claims 19 and 20, Bai discloses that if the first gate electrode is made of N-type material, the second electrode will be made of P-type material, and vice-versa. The first gate electrode material may include nickel or ruthenium oxide if the material is to have the work function of a P-type doped semiconductor or may include ruthenium if the material is to have the work function of an N-type doped semiconductor. The same is true for the second gate electrode. Hence, the first and second gate electrodes will be made of different conductive materials. See col. 1, ln. 42-54; col. 3, ln. 55 – col. 4, ln. 9; col. 4, ln. 41-53).

Regarding claim 21, Bai discloses that the first and second gate electrode materials may be made of nickel, ruthenium oxide or ruthenium (col. 1, ln. 41-53; col. 4, ln. 3-9; col. 4, ln. 42-53).

Regarding claim 22, Bai discloses that one of the gate electrodes may be made of a metal nitride (MoN) (col. 1, ln. 41-53).

Regarding claims 23 and 24, Bai discloses that the barrier layer may be TiN or TaN, both of which are conductive material (col. 3, ln. 51-54).

Regarding claims 27 and 28, Bai discloses that the barrier layer has a thickness of 5 – 200 (col. 3, ln. 36-37).

Regarding claim 33, Bai discloses depositing a layer of first gate electrode material (130 or 135 can be considered "a first gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 34, Bai discloses removing the first gate electrode material from over the second region without removing the underlying barrier layer (Fig. 5 and 7).

Regarding claim 35, in the event that the material 135 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by chemical mechanical polishing (col. 4, ln. 55-64).

Regarding claim 36, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 37, in the even that the material 130 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by differential etching (col. 29-33).

Regarding claims 38 and 41, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate and removing the second gate electrode material from over the first region without removing the underlying barrier layer (Fig. 5, 7 and 8).

Regarding claim 40, Bai discloses etching the barrier layer over portions of the second region to a thickness of 0 Angstroms (Fig. 8).

Regarding claim 42, Bai discloses depositing a dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the dielectric layer

such that it overlies both the first and second regions, depositing a first gate electrode material (130 or 135) over the first and second regions, removing the first gate electrode material from over the first region without removing the barrier layer, depositing a second gate electrode material (135 or 130), and defining a first and second electrode in the first and second regions.

Bai does not disclose by what method the gate dielectric layer and barrier layer may be deposited. Like Bai, Matsuse discloses depositing a gate barrier layer onto a gate dielectric layer. Matsuse teaches that it is advantageous to use atomic layer deposition (ALD) to deposit the gate dielectric layer and barrier layer because the ALD process allows the layers to be more densified than they would be if deposited by other methods and also allows the layers to be formed such that they are ultra-thin (Fig. 13A; col. 7, ln. 8-13; col. 19, ln. 20-52). Matsuse does not disclose that the barrier layer is a nanolaminate. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the barrier layer of Bai using an ALD process because Matsuse teaches that using ALD provides the benefits of forming densified, ultra-thin layers.

Regarding claims 43 and 44, Bai discloses that the barrier layer may be a ternary complex (TaSiN) (col. 3, ln. 51-54).

Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. in view of Matsuse et al. as applied to claim 15 above, and further in view of Pomarede et al. (US 20020098627).

Regarding claims 29-32, Bai discloses that the gate dielectric layer may be a high-k layer, but Bai does not disclose a method of forming the dielectric layer, nor treating the dielectric layer to remove OH groups. Pomarede teaches that it is advantageous to treat a layer such as a

high-k gate dielectric layer with a mixture including ammonia (nitrogen-hydrogen) plasma and nitrogen radicals upon which subsequent layers will be deposited (para. 84-90). This process inherently replaces OH groups on the surface of the high-k dielectric layer with nitrogen atoms. Pomarede states, "By changing the surface termination of the substrate [high-k dielectric] with a low temperature radical treatment, subsequent deposition is advantageously facilitated without significantly affecting the bulk properties of the underlying material." (Abstract). At the time of the invention, it would have been obvious to one of ordinary skill in the art to treat the surface of the gate dielectric film of Bai as is taught by Pomarede because Pomarede teaches that it is advantageous to change the surface termination of a high-k gate dielectric film that will have additional layers subsequently deposited thereon.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. in view of Matsuse et al. as applied to claim 15 above, and further in view of Chang et al. (US 6,660,630, previously cited).

Regarding claim 39, Bai does not disclose depositing a layer of conductive material over the first and second gate electrode layers. However, as is disclosed by Chang, it is necessary in the fabrication of semiconductor devices such as that of Bai, to deposit multi-layered conductive interconnection structures above the gates of a semiconductor device in order to provide required wiring to the gates of the device (col. 1, ln. 34-65). Such structures are well-known in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit conductive material over the first and second gate electrode layers of Bai for the purpose of forming a multi-layered interconnection structure that connects the gate with upper-level

wiring because such structures are necessary to the function of the gate and are well-known in the art.

Response to Arguments

Applicant's arguments with respect to claims 15-24 and 27-42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
August 22, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800